

SAMODYA ABEYSIRIWARDANE
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SUMMARY

- Generalist** with interests in **programming languages** / **dev tools** / **data intensive computing**

EDUCATION

MSc Computer Science – Purdue, West Lafayette, IN _____ Spring 2016–Fall 2018

- Workshop paper*: Mergeable Types, ICFP ML Workshop, 2017 – Contributed by implementing an OCaml AST transformer to auto derive 3-way merge functions for recursive data types
- Courses*: Distributed systems, Advanced database systems (Relational and non-relational), Programming Language Theory, Algorithm design and analysis

BSc Computer Engineering – Purdue, West Lafayette, IN _____ Fall 2011–Spring 2015

- Courses*: Circuit analysis, Computer design and prototyping, Signals and systems, Data structures and algorithms, Discrete Mathematics, Advanced C, Intro to AI, Intro to Infosec, Compilers, Operating Systems

MY ...

- Writeups** – <https://sransara.com/notes/>
- Open-source contributions** – <https://github.com/search?q=author:sransara+type:pr>

PROJECTS

- Play online multiplayer bughouse chess variation** *webrtc* – <https://utopia.buddychess.com/>
- Lay-zer playground** *typescript* – <https://github.com/sransara/lay-zers>
- SOCK5 Proxy** *go* – <https://github.com/sransara/odd-socks>
- Mergeable functional datastructures** *ocaml* – <https://github.com/sransara/mtypes-lib>
- Distributed key-value store** *java* – <https://github.com/sransara/kvs-transactions>
- Simple Compiler** *java* – <https://github.com/sransara/microbe-lang>
- Multicore MIPS processor** *verilog* – <https://github.com/sransara/aww-processor>

WORK

Hardware Engineer: Test Automation Developer – Cisco, San Jose, CA _____ June 2019–Present

- Building a test suite for validating circuit diagrams and PCB layouts to their specifications
- Mentor new team members on coding standards, best practices and version control
- To aid a refactoring project, develop a tool to convert some non-trivial Perl syntactic constructs to Python
- Experience with*: Python, Perl, SKILL (A Lisp for EDA tools), EDA tools, Agile process

Test Engineer – Jabil Circuit, San Jose, CA _____ Jan 2019–June 2019

- Develop a tab completer framework for an inhouse REPL, to build completers that improve debug workflow
- Extending the ETL pipeline, network tools, yield analysis tools for an HPC hardware emulation platform
- Experience with*: Go, Python, CI/CD, Design for testing in electronics mass manufacturing

Test Engineering Intern – Jabil Circuit, San Jose, CA _____ Summer 2018

- Building an ETL pipeline for live analysis of testcell grid data (*Jabil - Design Best Practices* competition)
- Experience with*: Data mining-visualization-analysis, Database design, Go, HTML/CSS/JS & React

Graduate Research Assistant – Computer Science, Purdue _____ Jan 2017–Dec 2018

- Worked on*: 3-way merging datastructures research project
- Explore mergeable functional datastructures and OCaml AST transformers (PPX)
- Experience with*: Database consistency and concurrency control, OCaml, Git internals

Undergraduate Teaching Assistant – Computer Engineering, Purdue _____ Jan 2015–April 2015

- Guide students in taking design decisions to develop a multicore pipelined MIPS processor
- Experience with*: Verilog, Logic synthesis on FPGA

Student Software Developer – Krannert Computing, Purdue _____ May 2012–Dec 2016

- Develop web and desktop apps. *Experience with*: C#, .NET, Database design, HTML/CSS/JS

OTHER

- Recognized in Google security hall of fame for disclosure of XSS bugs in Gmail: 2012 July, 2012 October